VIT-AP UNIVERSITY

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CoreEL Technologies — Enabling Excellence

Mentor A Siemens Business

ENTUPLE TECHNOLOGIES

cadence ACADEMIC NETWORK

2nd ONE WEEK WORKSHOP ON VLSI DEVICE, CIRCUIT AND SYSTEM DESIGN TOOLS (ONLINE)

Organized by

School of Electronics Engineering (SENSE), VIT-AP University

Date : 23rd June to 29th June 2022 (Thursday to Wednesday)

Limited Seats (60 Participants)

Registration is limited on the first-come-first-serve basis

Last date for Registration : 18th June 2022

About Our Workshop

The aim of this workshop is to provide an overview on EDA tools for VLSI design to the participants. The workshop will comprise of live demonstration of tools and lectures delivered by design engineers on platforms like Cadence, Tanner EDA, Calibre, Synopsys Sentaurus TCAD, Visual TCAD, Ngspice and Magic. This workshop is a generous attempt of qualified VLSI domain researchers to help and encourage the research scholars, undergraduate, postgraduate, and entrepreneurs to meet their research goals. The participants will have exposure to the state-of-the-art semiconductor devices to circuit modeling and integrated applications. After finishing this workshop, the participants will be able to execute the various analysis needed to characterize devices and circuits individually.

Who can attend : Faculty/UG/PG/Research scholars/Person from industry.

Platform: Online (Link will be provided after the registration)

Workshop Topics:

- Physical Unclonable Function (PUF) as the Hardware-Assisted Security (HAS) Primitive
- Demonstration of full-custom design using **Siemens Tanner EDA and Calibre**
- Live demonstration of **Visual TCAD from device to circuits**
- Demonstration of device simulation and analysis using **Synopsys Sentaurus 3D TCAD tool**
- Design of Ultra-High Speed SRAM Circuit by Efficient MOSFET Design with Electrical/thermal Co-optimization.
- Low power design and verification of digital system
- Static Power and Rail Analysis using **VOLTUS Tool (Cadence)**
- Dynamic Power and Rail Analysis using **VOLTUS Tool (Cadence)**
- Hands-on for performing ac, dc, and transient analysis of a circuit using **Ngspice**
- Hands-on experience in Layout design of a circuit using **Magic**

Highlights:

- Available Seats: **60** (first-come-first-serve basis)
- Last date of application: **18/6/2022**
- Intimation of selection: **20/6/2022**

◎ **REGISTRATION FEE: INR 500**

◎ **REGISTRATION & PAYMENT LINK (For External Participants):** Register through the link given below. The payment link is available inside the registration form. Pay the registration fee and upload the proof in the appropriate place

https://vtop1.vitap.ac.in/VLSICSDT/Conferenceinitial

◎ The **E-Certificate** will be provided to all the participants after successful completion of the workshop

AGENDA

Day-1 Thursday, 23nd June 2022

Session-I (10 am to 12 noon)

Prof. Saraju P. Mohanty
Professor, Department of Computer Science and Engineering, University of North Texas, Denton, US.

Session Talk :
Physical Unclonable Function (PUF) as the Hardware-Assisted Security (HAS) Primitive

Session-II (2 pm to 5 pm)

Mr. Shrinidhi P D
Application Engineer in CoreEL technologies

Session Talk :
Tool : Siemens Tanner EDA & Calibre

- Introduction to VLSI Design
- ASIC Design flow miniaturization techniques
- Demonstration on Full Custom Design with Tanner tool with SCL 180nm and performing PV with Calibre.

Day-2 Friday, 24th June 2022

Session-III (10 am to 12 noon)

Dr. V. Bharath Sreenivasulu
Assistant Professor, Department of ECE , MITS (AP)

Session Content :
Tool : Visual TCAD from device to circuits

- Design and simulation of 2D and 3D devices.
- Migration from device (Visual TCAD) to circuit(Cadence).

Session-IV (2 pm to 5 pm)

Dr. Rupam Goswami
Assistant Professor, Department of ECE, Tezpur University, Assam

Session Content :
Tool : Synopsys Sentaurus TCAD

- Design and simulation of 2D and 3D devices including interface trap charge and noise analysis.
- Design and simulation of devices for biosensor application.

Day-3 Saturday, 25th June 2022

Session-V (10 am to 12 noon)

Prof. Young Suh Song
Department of Computer Science
Korea Military Academy

Session Talk :
Design of Ultra-High Speed SRAM Circuit by Efficient MOSFET Design with Electrical/thermal Co-optimization

Session-VI (2 pm to 5 pm)

Mr. Murali Kilari
Design Engineer Manager, AMD

Session Content :

- Low power design and verification of digital systems

Day-4 Tuesday, 28th June 2022

Session-VII (10 am to 12 noon)

Mrs. Saraswati BP
PD Engineer for Cadence at Bangalore

Session Content :
Tool : Static Power and Rail Analysis using VOLTUS Tool (Cadence)

- Introduction to Power Analysis
- Voltus Library Generation
- Power analysis to Calculate Static Power
- Applying static power and piecewise linear current waveforms to control the power of particular instance
- Analyzing current/power plots
- Static Rail analysis to report IR / EM results
- Analyzing various rail analysis plots
- Tool Demonstration using Case Study

Session-VIII (2 pm to 5 pm)

Session Content :
Tool : Dynamic Power and Rail Analysis using VOLTUS Tool (Cadence)

- Voltus Library Generation
- Power analysis to Calculate Dynamic Power
- Setting toggle rates to nets
- Vector profiler for analyzing VCD files for windows with high activity, high average
- vpower, or high peak power
- Analyzing current/power plots
- Dynamic Rail analysis to report IR / EM results
- Analyzing various rail analysis plots
- Tool Demonstration using Case Study

Day-5 Wednesday, 29th June 2022

Session-IX (10 am to 12 noon)

Mr. Rahul Sharma
Research Scholar, Department of EEE,
IIT Guwahati

Session Content :
Tool : Ngspice

- Introduction to open source tools for VLSI chip design.
- Learn to write spice codes for simulating circuits.
- Introduction to “ngspice” tool. Hands-on for performing ac, dc, and transient analysis of a circuit using ngspice.

Note- Pre-Installation of ubuntu linux needed for hands on session.

Session-X (2 pm to 4 pm)

Session Content :
Tool : Magic

- Analog IC design complete flow from scratch.
- Introduction to “Magic VLSI layout” design tool.
- Hands-on experience in Layout design of a circuit with clean DRC

Note- Pre-Installation of ubuntu linux needed for hands on session.

Coordinators:

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