VIT-AP UNIVERSITY

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ASC

Academic Staff College

5-DAY WORKSHOP ON VLSI DEVICE AND CIRCUIT DESIGN TOOLS (ONLINE)

Organized by

School of Electronics Engineering (SENSE), VIT-AP University

Date : 22nd June to 26th June 2021 (Tuesday to Saturday)

Limited Seats (60 Participants)

Registration is limited on the first-come-first-serve basis

Last date for Registration : 18th June 2021

About Our Workshop

The aim of this workshop is to provide an overview on EDA tools for VLSI design to the participants. The workshop will comprise of live demonstration of tools and lectures delivered by design engineers on platforms like Cadence, Mentor Graphics, Xilinx, and Synopsys Sentaurus TCAD. This workshop is a generous attempt of qualified VLSI domain researchers to help and encourage the research scholars, undergraduate, postgraduate, and entrepreneurs to meet their research goals. The participants will have exposure to the state-of-the-art semiconductor devices to circuit modeling and integrated applications. After finishing this workshop, the participants will be able to execute the various analysis needed to characterize devices and circuits individually.

Who can attend : Faculty/UG/PG/Research scholars/Person from industry.

Platform: MS Teams

Workshop Topics:

- Introduction to Non-Classical MOS Transistor
- Live demonstration of device simulation and analysis using **Synopsys Sentaurus 3D TCAD tool**
- Physical Insights into the nature of Gate-induced Drain Leakage in Emerging Nano-scale FETs
- ASIC and full-custom design flow using **Synopsys tool**
- BACK-END design flow, generation of **GDS-II** and use of **Fin-FET library in Cadence**
- Static timing analysis using **Tempus** and clock tree synthesis concept in **Cadence**
- Demonstration of full-custom design using **Tanner tool**
- **Xilinx** FPGA design flow
- Demonstration on system generator flow with **Matlab**
- Demonstration on **PYNQ platform with Vivado**
- Introduction to **HDL Verification and UVM**
- Learn to build **UVM testbench** from scratch

Highlights:

- Available Seats: **60** (first-come-first-serve basis)
- Last date of application: **18/6/2021**
- Intimation of selection: **20/6/2021**

◎ **REGISTRATION FEE: INR 500**

◎ **REGISTRATION & PAYMENT LINK :** Register through the link given below. The payment link is available inside the registration form. Pay the registration fee and upload the proof in the appropriate place

https://forms.gle/SErtxdvFhfyvXJZB8

◎ The **E-Certificate** will be provided to all the participants after successful completion of the workshop

AGENDA

Day-1 Tuesday, 22nd June 2021

Session-I (10 am to 12 noon)

Dr. Satyabrata Jit
Professor, Department of Electronics Engineering, IIT BHU (PhD IIT BHU)

Session Talk :
Introduction to non-classical MOS Transistor

Session-II (2 pm to 5 pm)

Dr. Jegadheesan
Nanochip Solution (PhD)
(Currently working as a Post Doctoral Fellow in IIT Kanpur)

Session Content :
Tool : Live demonstration of Synopsys Sentaurus 3D TCAD

- Idea of simulating a device for its DC parameters, AC parameters, Mixed-mode analysis

Day-2 Wednesday, 23rd June 2021

Session-III (10 am to 12 noon)

Dr. Shubham Sahay
Assistant Professor,
Department of Electrical Engineering,
IIT Kanpur (PhD IIT Delhi)

Session Talk :
Physical Insights into the nature of Gate-induced Drain Leakage in Emerging Nano-scale FETs

Session-IV (2 pm to 5 pm)

Mr. Srinath BK
Design Manager, Nanochip Solution

Session Content :
Tool : Synopsys BackEnd

Day-3 Thursday, 24th June 2021

Session-V (10 am to 12 noon)

Mr. Navin Shankar
Application Engineer for Cadence
at Entuple Technologies (ME)

Session Contents :
Tool : Cadence
- Usage of Fin-FET library
- Complete Backend design flow from schematic to generation of GDSII

Session-VI (2 pm to 5 pm)

Mrs. Saraswati BP
PD Engineer for Cadence
at Bangalore (B.Tech)

Session Content :
Tool : Cadence
- Static timing analysis using Tempus
- Clock tree synthesis concept

Day-4 Friday, 25th June 2021

Mr. Ankur Sangal
Lead Application Engineer,
CoreEL Technologies (M.Tech)

Session-VII (10 am to 12 noon)

Session Contents :
Tool : Tanner EDA & Mentor Graphics
- Introduction of VLSI Design
- ASIC Design Flow Miniaturization techniques
- Demonstration on Full custom design with Tanner tool with SCL 180nm

Session-VIII (2 pm to 5 pm)

Session Contents :
Tool : Xilinx Vivado
- Introduction of Xilinx FPGA Design Flow
- 7 Series Architecture
- Demonstration on System Generator Flow with Matlab
- Demonstration on PYNQ platform with Vivado

Day-5 Saturday, 26th June 2021

Mr. Murali Kilari
Senior member technical staff,
Invecas (M.Tech)

Session-IX (10 am to 12 noon)

Session Contents :
Tool : Online EDA playground Introduction to HDL Verification and UVM
- UVM concepts and Architecture
- UVM Configuration Mechanism
- UVM Sequences and Phasing

Session-X (2 pm to 5 pm)

Session Contents :
Tool : Online EDA playground
- Difference between SV Testbench and UVM Testbench
- Learn to build UVM testbench from scratch

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In Association with : **Academic Staff College**
Prof. Samuel Johnson K, Asst. Director, ASC, VIT-AP University

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